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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,346	12/09/2003	Fang-Cheng Chen	TS02-1367	3543

42717 7590 09/20/2006

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,346	CHEN ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/26/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1, 3-10, 12-18 are stand rejected, claims 2, 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5, 7-8, 10, 12-14, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (U.S. Patent No. 6,025,242).

Referring to figures 1-6, Ma et al. teaches a method of forming a semiconductor device on a semiconductor substrate, comprising the steps of:

forming a high dielectric constant (high k) gate dielectric layer (2) on the semiconductor substrate (see figure 3); noted in the present invention page 5, lines 7-9, applicant refers silicon oxide is a high k layer.

forming a conductive gate (3) structure on a first area of the gate dielectric layer (2),

forming first insulator spacers (6) on the sides of the conductive gate structure (3) with the procedure used to form said first insulator spacers (6) also removing a second area of said gate dielectric layer (see figure 2-3), wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers (see figure 2-3),

forming a first doped region in an area of said semiconductor substrate not covered by conductive gate structure or by said first insulator spacers (8, see figure 4);

forming a second insulator spacers (10, see figure 6) on the sides of said first insulator spacers; and

forming a second doped region in an area (11, see figure 6) of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers (see figure 6).

Regarding to claims 3, 12, the thickness of the gate dielectric layer is between about 10-200 Angstroms (see col. 2, lines 23-25).

Regarding to claims 4, 13, the dielectric constant of said gate dielectric layer (silicon oxide) is greater than 4 (2, see col. 2, lines 18-25). It is inherent that the same material would provide the same dielectric constant.

Regarding to claims 5, 14, wherein said conductive gate structure is comprised of doped polysilicon at a thickness between about 300-3000 Angstroms (3, col. 2, lines 26-31).

Regarding to claims 7, 16, 17, first insulator spacers are comprised of silicon oxide, at a thickness between about 10 to 300 Angstroms (see col. 2, lines 54-58).

Regarding to claims 8, 16, 17, the first insulator spacers are comprised of silicon nitride, at a thickness between about 30 to 400 Angstroms (see col. 2, lines 54-58).

Regarding to claim 10, performing a dry etch procedure (reactive ion etch, see col. 2, lines 59-67) to first define first insulator spacers (6) on the sides of the conductive gate structure (3) via etching of said insulator layer, and then to remove exposed portions of the high gate dielectric layer, wherein said exposed portions of said high k gate insulator layer are portions not covered by said conductive gate structure or by said first insulator spacers (see col. 2, lines 59-67). Noted that in process of removing the insulating layer (5) to form the spacer (6), the insulating layer have to remove first before the removal of the gate dielectric layer (2) since the dielectric layer (2) is located below the insulating layer (5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,025,242) as applied to claims 1, 3-5, 7-8, 10, 12-14, 16-17 above in view of Ligon (U.S. Patent No. 6,630,721).

Ma et al. a method of forming gate transistor comprising a gate dielectric comprising silicon oxide, polysilicon gate electrode, and an insulating spacer formed by reactive ion etch. However, the reference does not teach the gate dielectric layer is comprised of a layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide.

Ligon teaches forming a high K gate dielectric layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide, silicon oxide (see col. 8, lines 61-67, col. 9, lines 1-17).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming the high k gate dielectric layer by using any of silicon nitride, tantalum oxide, silicon oxynitride instead of silicon oxide in process of Ma et al. as taught by Ligon because forming a high k dielectric gate would reduce leakage current.

Claims 6, 9, 15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,025,242) as applied to claims 1, 3-5, 7-8, 10, 12-14, 16-17 above in view of Bertrand et al. (U.S. Patent No. 6,841,449) and Komatsu (U.S. Patent Publication No. 2003/0011035).

Ma et al. a method of forming gate transistor comprising a gate dielectric, polysilicon gate electrode, and an insulating spacer formed by reactive ion etch. However, the reference does not teach etching the gate insulation layer and the dielectric layer to form spacer by using Argon and CF_4, and forming a gate electrode by using tungsten silicide instead of polysilicon.

Bertrand et al. teaches forming a gate dielectric layer (5) with the thickness of 25-50 Angstroms, forming a gate electrode (6), forming an insulation layer (7) and etching the

insulation layer (7) and the dielectric layer (5) by using Argon and CF_4 (see col. 2, lines 30-60, figures 1a-1b).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etch the gate insulation layer and the dielectric layer to form spacer by using Argon and CF_4 in process of Ma et al. as taught by Bertrand et al. because the process would provide high selective without overetch the bottom layer.

Komatsu teaches forming a gate electrode tungsten silicide (104) with the thickness of about 100nm=1000Angstrom.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would form a gate electrode by using tungsten silicide (104) with the thickness of about 100nm=1000Angstrom in process of Ma et al. as taught by Komatsu because the process would provide a low-resistance gate electrode, suited for a higher-speed operation of the semiconductor device.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-10, 12-18 are stand rejected, claims 2, 11 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that Ma et al. do not teach a high k gate layer. In response to applicant that Ma et al. clearly teach forming a high dielectric constant (high k) gate dielectric layer (2, silicon oxide, see col. 2, lines 18-25).) on the semiconductor substrate (see figure 3); noted in the present invention page 5, lines 7-9, applicant refers silicon oxide is a high k layer.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN